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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/922,990	08/03/2001	Stephen J. Keating	19570-05298	8457

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EXAMINER

NATNAEL, PAULOS M

ART UNIT	PAPER NUMBER
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2614

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/922,990	Applicant(s) KEATING ET AL.	
	Examiner Paulos M. Natnael	Art Unit 2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 June 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3,6-10,13-15,18-20 and 23-51 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-3,6-10,13-15,18-20 and 23-40 is/are allowed.
- 6) ☒ Claim(s) 41-43 and 46 is/are rejected.
- 7) ☒ Claim(s) 44,45 and 47-51 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Objections

1. Claims **47-49** are objected to under 37 CFR 1.75 as being a substantial duplicate of claims **13-15**. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).
2. Claims **50** and **51** are also objected by being dependent on objected claim 47.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim **41-43,46** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al., U.S. Patent No. 6,088,323

Considering claim **41**, Kobayashi et al disclose all claimed subject matter, note;

a) a rising edge corrector to receive jittered signal and to output a jitter corrected

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rising edge of the jittered signal, is met by the Rising Edge Correction circuit 17A, fig.1;

b) a falling edge corrector to receive the Jittered signal and to output a jitter corrected falling edge of the jittered signal, is met by the Falling Edge Correction circuit 17B, fig.1;

c) an output device to receive the jitter corrected rising edge, to receive the jitter corrected falling edge, and to output a jitter corrected signal, is met by Flip/Flop 25, fig.1, which receives the SS and SR signals and outputs an S5 signal. ((see also col. 5, line 1 to col. 6, line 10)

Except for;

d) wherein the jittered signal further comprises a deserialized signal derived from a serialized signal;

Regarding d), Serialization is a process of transmitting coded characters on bit at a time. Kobayashi et al do not specifically disclose a deserializing a serialized signal. However, Kobayashi et al discloses on col. 3 line 65 through col. 4, line 8 that "The audio data D1 is inputted from the digital audio tape recorder 3 to a modulation circuit 13. In addition, subcode data corresponding to the audio data D1 is inputted to the modulation circuit 13. The modulation circuit 13 conducts data processing on the audio data D1 and the subcode data by using a data processing scheme stipulated for a compact disk. In other words, the modulation circuit 13 adds error correction codes to the audio data D1 and the subcode data, thereafter conducts interleave processing thereto, subsequently conducts an EFM modulation, and outputs an EFM signal S2."

Therefore, it would have been obvious to the skilled in the art to modify the system of Kobayashi by providing a deserializer to deserialize the signal which has been coded with audio/video data, so that the output signal would be smoother without flutter or jitter.

Considering claim **42**, the apparatus of claim 1 wherein the rising edge corrector further comprises a rising edge detector to receive the jittered signal and to detect a rising edge of the jittered signal, wherein the falling edge corrector further comprises a falling edge detector to receive the jittered signal and to detect a falling edge of the jittered signal, is implied because the corrector would not be able to correct the rising and falling edge signals without first detecting or determining the position or other characteristics of the signals. (see also Figs.2A-D and 3)

Considering claim **43**, the apparatus of claim 1 wherein the rising edge corrector further comprises a rising edge adjuster to receive the jittered signal and to adjust a rising edge of the jittered signal; and wherein the falling edge corrector further comprises a falling edge adjuster to receive the jittered signal and to adjust a falling edge of the jittered signal, is inherent in the edge correction circuits 17A and 17B, because correcting implies or entails somehow adjusting the rising edge and falling edge signals. (see col. 5, lines 1-9 as well)

Considering claim **46**, the apparatus of claim 1, wherein the Jittered signal further comprises a video signal.

Regarding claim 46, Kobayashi discloses optical disk recording device and method. Optical disks such as compact disc or the DVD are well known for storing both audio and video signals. Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Kobayashi et al by providing video signal in the optical disk recording in order for the system to be able to correct jitter in the video signal as well, so that the system is made versatile and more useful for the consumer.

Allowable Subject Matter

5. Claims **1-3,6-10, 13-15,18-20, 23-40** are allowable over the prior art.
6. Claims **44,45** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
7. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose an apparatus comprising a counter to receive a base signal and to output a count of the base signal; a rising edge corrector to receive jittered signal and to output a jitter corrected rising edge of the jittered signal, wherein the rising edge corrector is configured to correct a rising edge of the jittered signal using the count received from the counter; a falling edge corrector to receive the Jittered

signal and to output a jitter corrected falling edge of the jittered signal; wherein the falling edge corrector is configured to correct a falling edge of the jittered signal using the count received from the counter; an output device to receive the jitter corrected rising edge, to receive the jitter corrected falling edge, and to output a jitter corrected signal, as in claim 1; receiving a jittered signal; determining a count of a current duration of a base signal; correcting a rising edge of the jittered signal; wherein correcting a rising edge further comprises using the count to correct the rising edge; correcting a falling edge of the jittered signal, and outputting a jitter corrected signal using the corrected rising edge and the correct falling edge, as in claims 13 and 18;

Wherein the falling edge corrector is configured to correct a falling edge of the Jittered signal using the count received from the counter, a rising edge position adjuster to receive the detection of the rising edge from the rising edge detector, to receive the count from the counter, to determine a rising edge count, to determine whether the rising edge count is within a programmed rising edge window, and to output a center position of the rising edge window as a jitter corrected rising edge position; and, a falling edge position adjuster to receive the detection of the falling edge from the falling edge detector, to receive the count from the counter, to determine a falling edge count, to determine whether the falling edge count is within a programmed falling edge window, and to output a center position of the falling edge window as a jitter corrected falling edge position; a jitter corrected signal output device to receive the jitter corrected rising edge position from the rising edge position adjuster, to receive the jitter corrected falling edge position from the falling edge position adjuster, and to output the jitter corrected

rising and falling edges as a jitter corrected signal by using the count from the counter, as in claim **23**;

A counter to receive a base signal and to output a count of the duration of the base signal; a rising edge corrector to receive the jittered signal, to receive the count from the counter, to determine a rising edge count, to output the rising edge count as a jitter corrected rising edge position of the jittered signal if the rising edge count is not within a rising edge programmed window, and to output the center of the rising edge programmed window as the jitter corrected rising edge position of the jittered signal if the rising edge count is within the rising edge programmed window; falling edge corrector to receive the jittered signal, to receive the count from the counter, to determine a falling edge count, to output the falling edge count as the jitter corrected falling edge position of the jittered signal if the falling edge count is not within a falling edge programmed window, and to output the center of the falling edge programmed window as the jitter corrected falling edge position of the jittered signal if the falling edge count is within the falling edge programmed window; and a jitter corrected signal output device coupled to receive the jitter corrected rising edge position from the rising edge corrector, to receive the jitter corrected falling edge position from the falling edge corrector, and to output a jitter corrected signal, as in claim **28**;

Counting a duration of a base signal, when a rising edge of the jittered signal occurs, determining a rising edge count based on the count of the duration of the active state of the base signal; determining whether the rising edge count is within a rising

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edge window; if the rising edge count is within a rising edge window, then outputting the center of the rising edge window as a jitter corrected rising edge position or otherwise outputting the rising edge count as the jitter corrected rising edge position; when the falling edge of the jittered signal occurs, determining a falling edge count based on the count of the duration of the active state of the base signal; determining whether the falling edge count is within a falling edge window; the falling edge count is within a falling edge window, then outputting the center of the falling edge window as a jitter corrected falling edge position or otherwise outputting the falling edge count as the jitter corrected falling edge position; outputting a jitter corrected signal by matching the count from the counter with the respective jitter corrected rising edge and falling edge positions, as in claim 34;

Conclusion

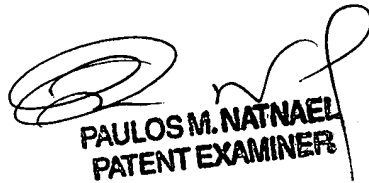
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PMN
December 5, 2004



PAULOS M. NATNAEL
PATENT EXAMINER